PHYSICS OF FAILURE MODELS FOR CAPACITOR DEGRADATION IN DC-DC CONVERTERS

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Abstract

This paper proposes a combined energy-based model with an empirical physics of failure model for degradation analysis and prognosis of electrolytic capacitors in DC-DC power converters. Electrolytic capacitors and MOSFET's have higher failure rates than other components in DC-DC converter systems. For example, in avionics systems where the power supply drives a GPS unit, ripple currents can cause glitches in the GPS position and velocity output, and this may cause errors in the Inertial Navigation (INAV) system causing the aircraft to fly off course. We have employed a topological energy based modeling scheme based on the bond graph (BG) modeling language for building parametric models of electrical domain systems. Our current work adopts a physics of failure model (Arrhenius Law) for equivalent series resistance (ESR) increase in electrolytic capacitors subjected to electrical and thermal stresses. Experiments for capacitor degradation were conducted for collecting degradation ESR data. Parameter re-estimation for the failure model is done using the experimental data. The derived degradation model of the capacitor is reintroduced into the DC-DC converter system model to study changes in the system performance using Monte Carlo simulation methods. Stochastic simulation methods applied to the combined model help us predict how system performance deteriorates with time.

Key words: Bond graphs; DC-DC converters; ESR; Electrolytic capacitors; Diagnostics; GPS; INAV; prognostics; health management

Introduction:

Electrolytic capacitors and MOSFET's have higher failure and degradation rates among all of the components in DC-DC converter systems. The failure in these components can be attributed to a variety of factors, such as High Voltage conditions, Transients, Reverse Bias, Strong Vibrations and high ripple current. Degraded capacitors affect the performance and efficiency of the DC-DC converters in a significant way. The paper develops a method for studying the degradation effects of electrolytic capacitors subject to ripple currents, and their impact on overall system performance.

This paper proposes an energy-based approach to modeling nominal system behavior combined with physics of failure models to represent component degradation of electrolytic capacitors. The models form the core of simulation-based methods for prognostic and degradation analysis of performance in DC-DC power converters in aircraft avionics systems. The output degradation in the DC-DC converters is typically measured by the increase in ripple current and the drop in output voltage at the load. Typically

the ripple current effects dominate, and they can have adverse effects on downstream components. The work in this paper is specifically related to DC-DC converters in Avionics systems. In these systems the power supply drives a GPS unit, and ripple currents at the converter output can cause glitches in the GPS position and velocity output, and this, in turn, may cause errors in the Inertial Navigation (INAV) system causing the aircraft to fly off course.

A model based approach to studying degradation phenomena enables us to combine energy based modeling of the DC-DC converter with physics of failure models of capacitor degradation to predict the health of the system using stochastic simulation methods. The simulations provide quantitative evaluations of how the system performance deteriorates with time. A topological energy based modeling scheme based on the bond graph (BG) modeling language is employed for building parametric models of electrical domain systems. The BG approach captures relationship between component parameters, system behavior, and performance, and provides a systematic and accurate methodology for linking component degradations with deterioration in system performance over time. This deterioration, when mapped to suitable metrics provides the basis for establishing the remaining useful life (RUL) of the capacitor components, and, therefore, for the converter system.

In particular, this paper studies the effects of capacitor degradation on DC-DC converter performance using our model-based methodology when the electrolytic capacitors are subjected to thermal and electrical stresses. The capacitor component degradation models are constructed using empirical physics of failure phenomena, which express as mathematical relations the temporal changes in component parameters due to the applied stressors. The stressors can be thermal when the capacitors operate in high temperature environments, and electrical due to high operating voltages (at or above the specified max for the capacitor) and ripple currents that exceed the rated maximums. In our work, we use data from experimental runs to validate and establish the parameters of the physics of failure models for the capacitors.

Our physics of failure model (Arrhenius Law) in electrolytic capacitors captures the increase in the Equivalent Series Resistance (ESR) when the capacitors are subjected to electrical and thermal stresses. To study the degradation effect, degraded models of the capacitors are reintroduced into the DC- DC converter system model to study changes in the system performance using Monte Carlo simulation methods. The simulation results observed under different stress conditions are validated using experiments we have run in a lab at NASA Ames. The experimental results are used the verify a model of capacitor degradation reported in the literature (Venet and Grellet, 1993), and to derive more accurate parameter values of the particular brands of capacitors that are employed in our DC-DC converters. The degraded capacitor model is then introduced into the DC-DC converter model, and using Monte Carlo simulations used to predict the loss in converter performance over time.

The rest of this paper is organized as follows. The next section describes in detail the DC-DC converter model. In the following section we discuss the mechanisms for degradation in DC-DC converters and review capacitor degradation models. We study the DC-DC converter model and discuss the capacitor degradation in the model. The next section discusses the degradation experiments conducted on electrolytic capacitors and compare the simulation data with the experimental data. This helps refine the model parameters, verify the validity of the empirical models, and then employ the validated models to predict the loss in DC-DC converter performance over time. The paper concludes with discussion of the results and future work.

DC-DC CONVERTERS:

Switched-mode power supplies are widely used in DC-DC converters because of their high efficiency and compact size. DC-DC converters are important in portable electronic devices, which derive their power

primarily from batteries. Such electronic devices often contain several sub-circuits with different voltage requirements (sometimes higher and sometimes lower than the supply voltage, and possibly even negative voltage). DC-DC converters can provide additional functionality for boosting the battery voltage as the battery charge declines.

A typical buck-boost DC-DC converter circuit is illustrated in Fig. 1. Such converters step the voltage up or down, by storing the input energy temporarily in inductors when switch sw1 is ON and switch sw2 is OFF, and then releasing that energy to the output at a different voltage value when sw2 is ON and sw1 is turned OFF. The efficiency of conversion ranges from 75% to 98%. This high efficiency is typically achieved by using power MOSFET's (metal oxide semiconductor field-effect transistor), which can provide high frequency switching more efficiently than power bipolar transistors, which, in addition to greater switching losses require more complex drive circuits. Overall, MOSFET switches increases the battery life in such devices. A buck boost approach is used for conversion to the required dc voltage output. Our particular application has an input of 28V DC from a battery source, and the required output voltage is 5V. The switches sw1 and sw2 are power MOSFET's, which are controlled by an external controller. Fig. 2 shows the external controller box, which controls the switching of the MOSFET's to maintain the required output voltage. We use the Bond Graph modeling paradigm (Karnopp and Rosenberg, 1983) for modeling the DC-DC converter.

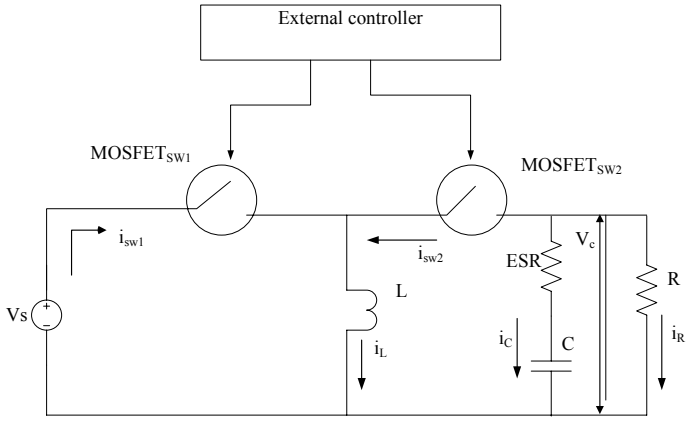

Figure 1: Buck Boost Converter Circuit

We develop a systematic approach for reliable diagnostics and prognostics for the converter system. For this we need to capture the topological and functional dependence of the system in addition to component level faults and capturing the causal flow in time to account for transient failures. The bond graph modeling paradigm provides the framework for building the system models from components. A detailed description of the bond graph models for the DC-DC converter and capacitor are discussed in the next section.

Bond Graph Modeling: Model-based identification methodologies require system models that accurately represent system dynamics and are also capable of linking system measurements to damage in the components of the model. The bond graph (BG) modeling framework provides both these features (Karnopp and Rosenberg, 2000). BGs provide a systematic framework for lumped parameter modeling across multiple domains that include the electrical, mechanical, hydraulic, and thermal domains (Gawthrop and Smith, 1996; Dragan, Antic, and Mladenovic, 1999). They are an explicit topological modeling language for capturing the dynamic energy transfer among components of a systems based on the principles of continuity of power and conservation of energy.

This energy distribution reflects the history of the system and, therefore, defines its state at a point in time. Behavior of the system at future time points is determined by the current state description and subsequent input to the system (Dragan, Antic, and Mladenovic, 1999). Changes in the state of the physical system are related to energy exchange among its components, which can be expressed in terms of power. The basic working principle of bond graphs is that power transmitted between connected components can be expressed as a product of 'effort' and 'flow', irrespective of the application domain (Gawthrop and Smith, 1996).

Table 1: Basic Bond graph elements

Symbol	Type of element	Name of element	Electric Domain
C	storage	capacitance	capacitor
L		inductance	inductor
R	dissipator	resistance	resistor
TF	transducer	transformer	transformer
GY		gyrator	
Se	source	effort source	voltage source
Sf		flow source	current source
1	junction	1-junction	series connection
0		0-junction	parallel connection

Bond graph elements are classified into one of five basic elements, (1) energy storage elements, Capacitance (C), the Inertia (I), (2) the dissipative element, Resistor (R), (3) two idealized energy transformation elements, the transformer (TF) and the Gyrator (GY), (4) two source elements, *Se*, source of effort and *Sf* , source of flow, and (5) two junction elements, 0 (for parallel connections) and 1 (for series connections). All these elements exchange energy with other elements through ports or bonds. Bonds are energy transfer pathways that connect elements and junctions and are represented as half arrows. Effort and flow signals are the information transferred through these pathways. The two ideal source elements model energy flow in and out of a system, and are active elements since they introduce energy into the system. All the other elements are passive.

DC-DC converter model: A passivity based approach discussed in (Garcia-Gomez *e*t *al.*, 2006) is used for deriving the BG model of the buck boost converter. This approach models the system behavior in two stages: (i) an energy shaping stage, where the closed loop total energy of the system is modified, and (ii) a damping injection stage, where the required dissipation is added in order to achieve asymptotic stability. The bond graph of the passivity based buck boost converter model is shown in Fig. 2. Se:Vs is the battery voltage. The switching elements sw1 and sw2 are replaced by modulating transformers (MTFs).

The representation of the switching devices as MTFs is derived directly from the algebraic relations of the effort and flow variables. In an average model of the buck-boost converter, the switching bond is replaced by a 'duty-ratio-modulated bond'. This 'average' bond can be effectively interpreted as an ideal lossless transformer with turns ratio specified by the complementary duty ratio function associated with the controlling scheme. The switching frequency of the MTFs depends upon the value α. The value of α is calculated from the values of R2, C, L and the input/output voltage requirements. (Garcia-Gomez *e*t *al.*, 2006) provides the detailed equations used for deriving the value of α.

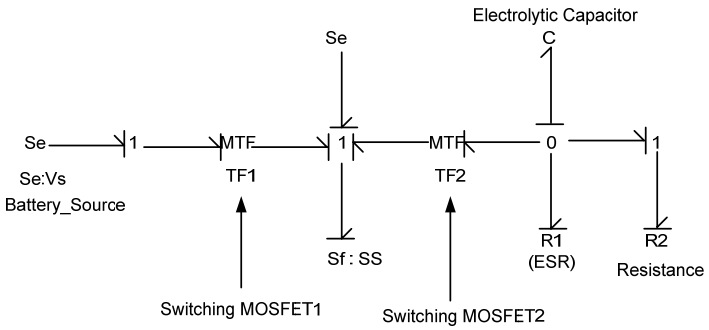

Figure 2: Buck Boost Converter Bond Graph Model

The regulation of the converter output at a desired output voltage v_{Cd} depends on the steady state value of the average inductor current i_L. This is determined by replacing dynamic element L (inductor) of the average bond graph by a SS-element (source-sensor element), represented as flow source Sf in the BG. The desired steady state value for the current can then be obtained as $i_L = (1 + v_{Cd}/vs)v_{Cd}/R2$. An input injection from the external passivity controller to the modulated effort source is added to the bond graph model of DC-DC converter in the form of a Se element. (Garcia-Gomez *et al.*, 2006) provides more details.

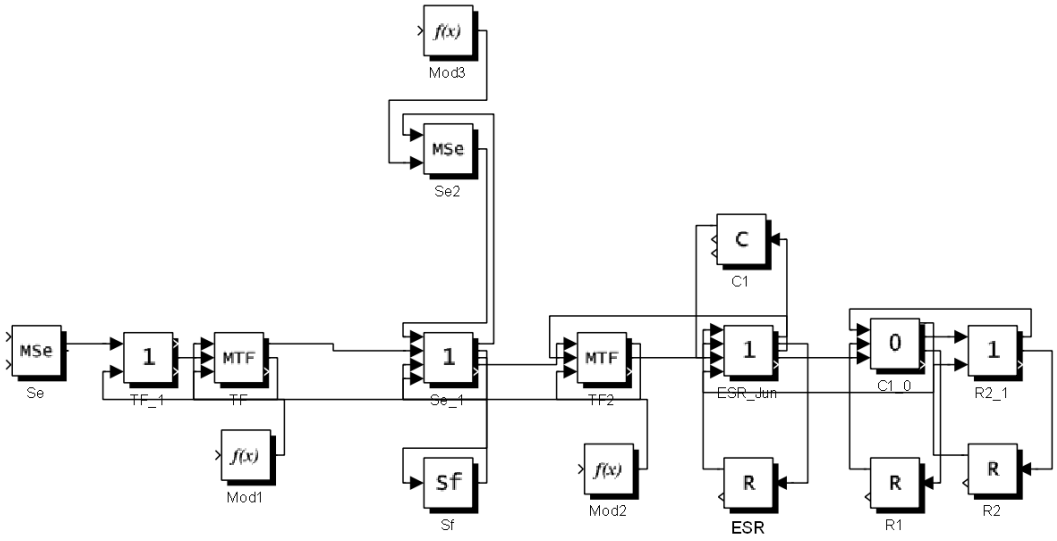

Figure 3: Buck Boost Converter Simulink Model

For conversion of the topological bond graph model to its equivalent MATLAB/ SIMULINK® model we use the approach presented in (Roychoudhury *et al.*, 2009). An interpreter is used for converting the BG model into an intermittent block diagram model from which the simulation model is derived. In its first stage, the interpreter navigates through the model hierarchy, mapping all the BG elements to block diagram (BD) elements. The second stage of the interpretation process consists of generating the simulation components from the BD model. The BD has all the required information for generating the simulation model. The generated simulation model from the BG model is shown in Fig. 3. Once the MATLAB/ SIMULINK® model is generated, the required simulation results for the DC-DC converter can be observed under different operating conditions. Our approach in the paper is to run degradation

experiments on capacitors and use the results to validate an empirical capacitor degradation model reported in the literature. In addition, we will also derive more accurate parameter values for the capacitors employed in our DC-DC converter system, and, therefore, generate better estimates of converter degradation over time.

Component Degradation/Failure: It has been reported in the literature that electrolytic capacitors are the leading cause for breakdowns in power supply systems (Imam *et al.*, 2005). The performance of the electrolytic capacitor is strongly affected by its operating conditions, which includes voltage, current, frequency, and working temperature. For degraded electrolytic capacitor the impedance path for the ac current in the output filter keeps increasing, thus introducing a ripple voltage on top of the desired DC voltage. Continued degradation of the capacitor leads the converter output voltage to also drop below specifications and in some cases the combined effects of the voltage drop and the ripples may damage the converter itself in addition to affecting downstream components. The detailed analysis for prognosis is carried out in several steps. These are outlined in the next section

ELECTROLYTIC CAPACITOR DEGRADATION:

This section discusses in detail the conditions under which the capacitor degrades leading to faults in the system. We study the adverse effects of ripple currents, which cause degradation by raising the temperatures in the capacitor core.

Physical Model of the Capacitor: An aluminum electrolytic capacitor, illustrated in Fig. 5 consists of a cathode aluminum foil, electrolytic paper, electrolyte, and an aluminum oxide layer on the anode foil surface, which acts as the dielectric. When in contact with the electrolyte, the oxide layer possesses an excellent forward direction insulation property. Together with magnified effective surface area attained by etching the foil, a high capacitance is obtained in a small volume (Fife, 2006).

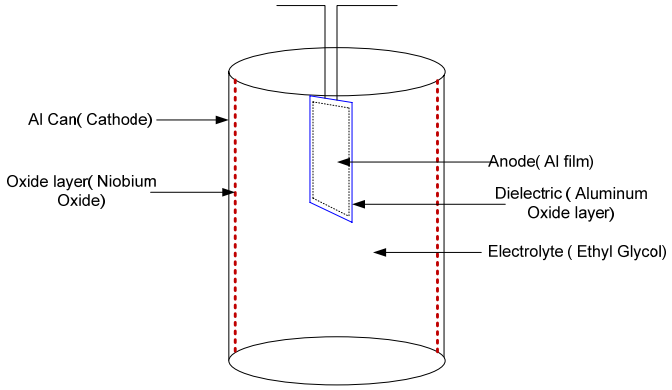

Figure 5: Physical Model of Electrolytic Capacitor.

Since the oxide layer has rectifying properties, a capacitor has polarity. If both the anode and cathode foils have an oxide layer, the capacitors would be bipolar. In this paper we analyze 'non-solid' aluminum electrolytic capacitors in which the electrolytic paper is impregnated with liquid electrolyte. There is another type of aluminum electrolytic capacitor, that uses solid electrolyte but we will not referring to these types in this work (Fife, 2006; Bengt, 1995).

Degradation Mechanisms: There are several factors that cause degradation in electrolytic capacitors. The degradation over a period of time finally results in the failure of the component, which impacts the working of the subsystems that are part of the overall system. The definition of failure and some of the failure modes are discussed below.

Failures in a capacitor can be one of two types: (1) catastrophic failures, where there is complete loss of functionality due to a short or open circuit and (2) degradation failures, where there is gradual deterioration of capacitor function. Degradation failures are related to an increase in the equivalent series resistance (ESR) and decrease in capacitance over time. Capacitor degradation is typically attributed to:

1. High Voltage conditions: The capacitance decreases and ESR increases.
2. Transients: The leakage current can be high and an internal short-circuits can occur.
3. Reverse Bias: The leakage current becomes high with loss of capacitance and increase in ESR.
4. Strong Vibrations: These can cause internal short circuits, capacitance losses, high leakage currents, increase in ESR and open circuits.
5. High Ripple current: These cause internal heating, increasing the core temperature which results in gradual aging of the capacitor.

The wear out of aluminum electrolytic capacitors is due to vaporization of electrolyte that leads to a drift in the main electrical parameters of the capacitor. One of the primary parameters is the equivalent series resistance (ESR). The ESR of the capacitor is the sum of the resistance due to aluminum oxide, electrolyte, spacer, and electrodes (foil, tabbing, leads, and ohmic contacts). The health of the capacitor is often measured by the ESR value. Over the operating period, the capacitor degrades i.e. its capacitance decreases and ESR increases. Depending upon the percentage increase in the ESR values we can evaluate the healthiness of the capacitor. Considering the current ESR value and operating conditions the remaining useful life of the capacitor can be calculated using model-based methods. There are certain industry standards for these parameter values, if the measurements exceed these standards then the component is considered failed, i.e., the component has reached its end of life, and should be immediately replaced before further operations. The next section discusses in detail the physics of failure models used to represent the degradation process in electrolytic capacitors.

Physics of Failure Models for Capacitor Degradation: Life prediction (Lahyani et al., 1998) and Failure prediction (Chen, 2005) are the two methods used to model electrolytic capacitor degradation. Depending upon the value of ESR, the remaining useful life (RUL) of the capacitor can be predicted for a given operating period under specific operating conditions. In the Life prediction method, ESR is calculated considering the increase in the temperature due to the ripple current, while in the Failure prediction method the ESR is calculated from the variations in output voltage and current of the DC-DC converter. In this work, we focus on the Life prediction method to study the effects on ripple current on capacitor degradation.

Life Prediction Method: Typically, thermal degradation affects both the capacitance and ESR values of electrolytic capacitors. (Lahyani et al., 1998; Chen, 2005) report on the change in ESR values due to thermal degradation. A linear inverse model (Venet and Grellet, 1993) has been derived as an extension of Arrhenius Law to define the change in ESR value over time for a capacitor subjected to a constant high temperature. The linear inverse model for computing is given by:

$$\frac{1}{ESR_t} = \frac{1}{ESR_0}(1 - k.t.exp(\frac{-4700}{T + 273}))$$

where:

- ESR_t = the ESR value at time ‘t’.
- T = the temperature at which the capacitor operates.
- t = the operating time.
- ESR_0 = initial ESR value at t = 0.
- k = constant which depends on the design and the construction of the capacitor.

The factor k depends on capacitor geometry and size. The value of k is typically determined empirically for a particular class of capacitors. For the simulation study below, we use k values reported in the literature, but we will conduct experiments to determine the value of k in future work.

CAPACITOR DEGRADATION EXPERIMENTS:

We ran degradation experiments for 650 hours of operation time. This long experiment was conducted to determine capacitor degradation in DC-DC converters when working at room temperature and long operating time. The DC-DC converter used for the experiments was purchased off the shelf, which met the specifications for the experiment. Under nominal conditions, the DC-DC converter has a variable input from 22V-36V DC and gives an output of 5V with 1% ripple and noise. Figure 7 shows the hardware used for the experiment. The configuration for the experimental hardware matches the schematic of the DC-DC converter presented earlier. The main hardware components include the MOSFETs, isolating transformers, pulse width modulation (PWM) controller chip and the filter electrolytic capacitor at the output. The capacitor (shown by a pointer in Fig. 7) is subjected to stresses that occur due to long operations at room temperature.

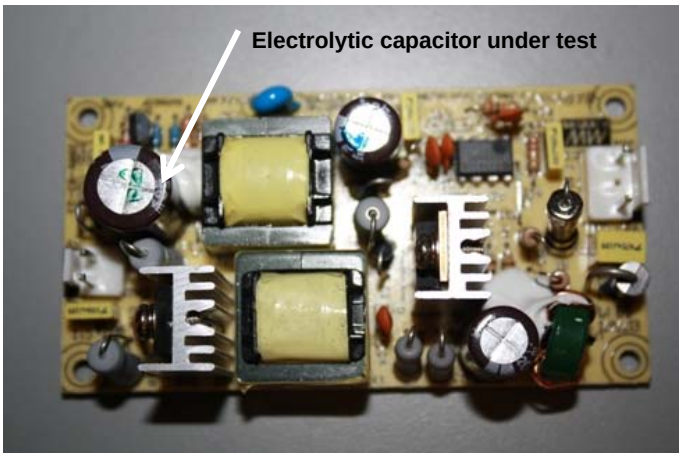

Figure 7: DC-DC converter hardware used for the experiment.

In this experiment we recorded the capacitor degradation under normal operating conditions for degradation over the period of time. The next sections discuss the experimental setup in detail.

DC-DC converter Electrical Stress Setup: Three sets of DC-DC converter hardware were considered for the experiment as discussed earlier. The electrolytic capacitors under test were measured for the initial ESR value before the start of the experiment at room temperature. The ESR was measured using an SP-150 Bio-logic measuring instrument. The average initial ESR value was measured to be 50mΩ for the three electrolytic capacitors under test. Figure 8 shows the setup used for the experiment.

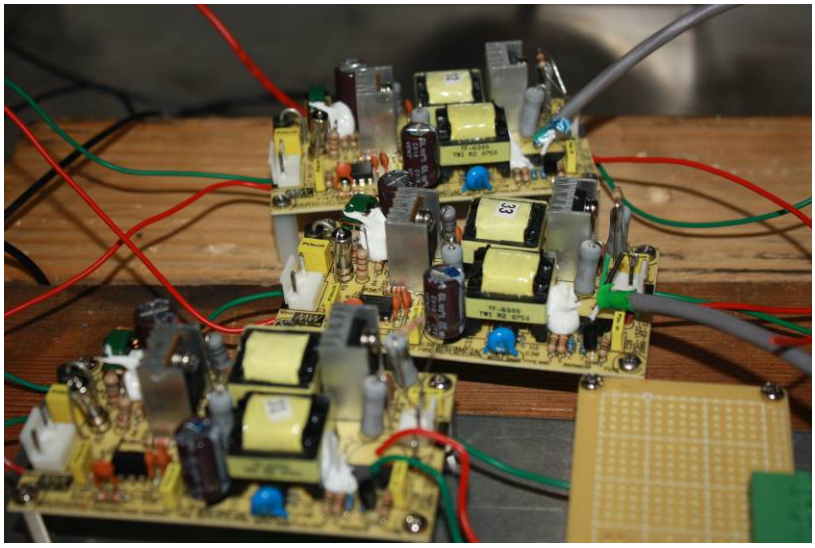

Figure 8: Experimental Setup.

The input DC voltage is supplied from a steady voltage source. A constant input voltage of 22V was supplied to the converter. At the output the voltage was observed which gave a constant value 5V with the ripples of accepted noise tolerance. In all three DC-DC converters were put under test at the same time, and the measurements for all the three capacitors on these converters were done accordingly. This is shown in the figure 9 which shows the digital oscilloscope output for one of the DC-DC converters. The ESR measurements were made approximately every 100-150 hours. The ambient temperature for the experiment was kept at 25°C in a controlled chamber such that the temperature was kept constant during the entire period of the experiment. During each measurement the voltage source was shut down, the capacitor was discharged completely and measurements for the ESR were taken. This was done for all the capacitors under testing. Keeping all the conditions intact the experiment was started again till the next measurement.

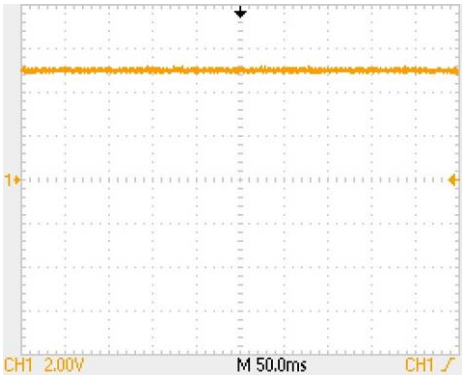

Figure 9: Output Voltage of the DC-DC converter on the Digital Oscilloscope.

Experiments for all the three DC-DC converters were conducted for a total of 650 hours of operation each. Measurements for the ESR of each of the capacitors under test were made at regular intervals. Table 4 shows the average percentage increase in the ESR value of the electrolytic capacitors. From the table we observe that the increase in the ESR value at the end of 650 hrs was observed to have increased by 12% - 13% of the initial ESR value, which was 0.0411 mΩ at the start of the experiment.

Table 4: Percentage Increase in ESR in Experiment Setup at Room Temperature (25^0C).

Time in Hours	Average % Increase in ESR Value
0	0
150	1.9
250	3.89
300	6.15
350	6.32
500	8.94
650	12.23

VALIDATION OF EXPERIMENTAL DATA AND PARAMETER ESTIMATION:

The measured experimental data was used for computing the model parameter 'k', and then using the validated model to show the loss in DC-DC converter performance over time. To demonstrate the inverse linear relation between ESR increase and time, we plotted $\frac{1}{ESR_t} - \frac{1}{ESR_0}$ against time as shown in Figure 11.

The least squares fit curve was used to re-estimate the value of the constant parameter 'k' as the slope of least squares fit line is shown in Figure 11. The least square error of the best fit line provides the possible variation in the value of slope, and the uncertainty in the 'k' value, and, therefore, the distribution of the ESR values is computed from the least squares error. The computed value of 'k' for these set of capacitors is 1.77± 0.1388, which is within the range of [1 2] reported in the literature.

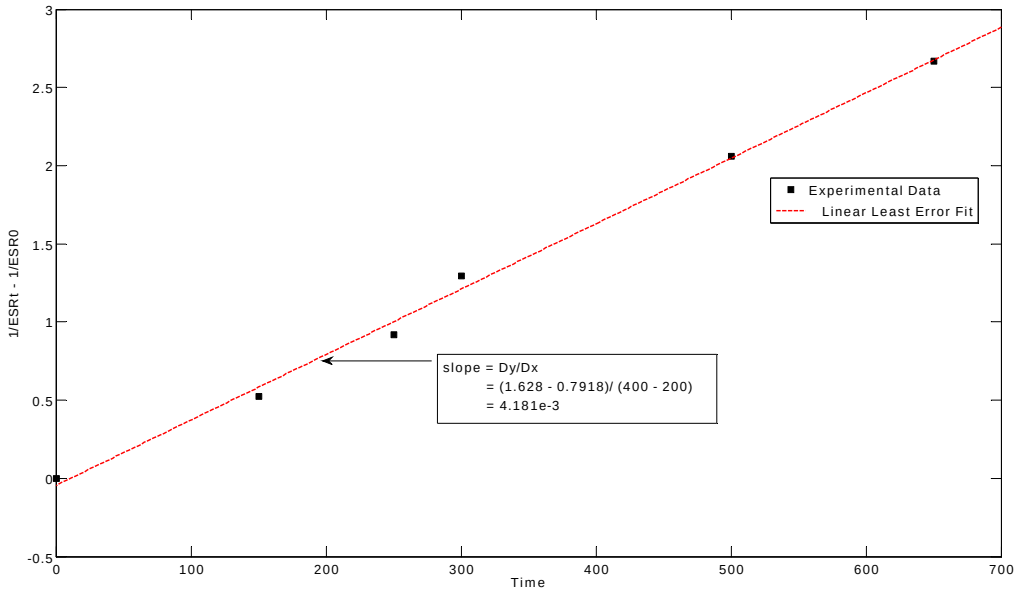

Figure 11: Re-estimation of 'k'

Using the estimated value of parameter 'k' we performed Monte Carlo simulations to determine the output performance of the DC-DC converter model taking into account the capacitor degradation, which produced the increase in ESR. The Life prediction model described earlier was used, and a normal distribution, using the computed mean and the variance determined from the experimental analysis, was used to represent the variation in parameter 'k', and, therefore, the ESR. The converter performance was computed assuming that it was operating at a steady temperature of 30°C under normal operating conditions (the same conditions under which the experiment to determine 'k' was conducted). Figure 12 shows the percentage increase in the RMS value of the ripple voltage at the output as the ESR value of the degraded capacitor increases over the period of time.

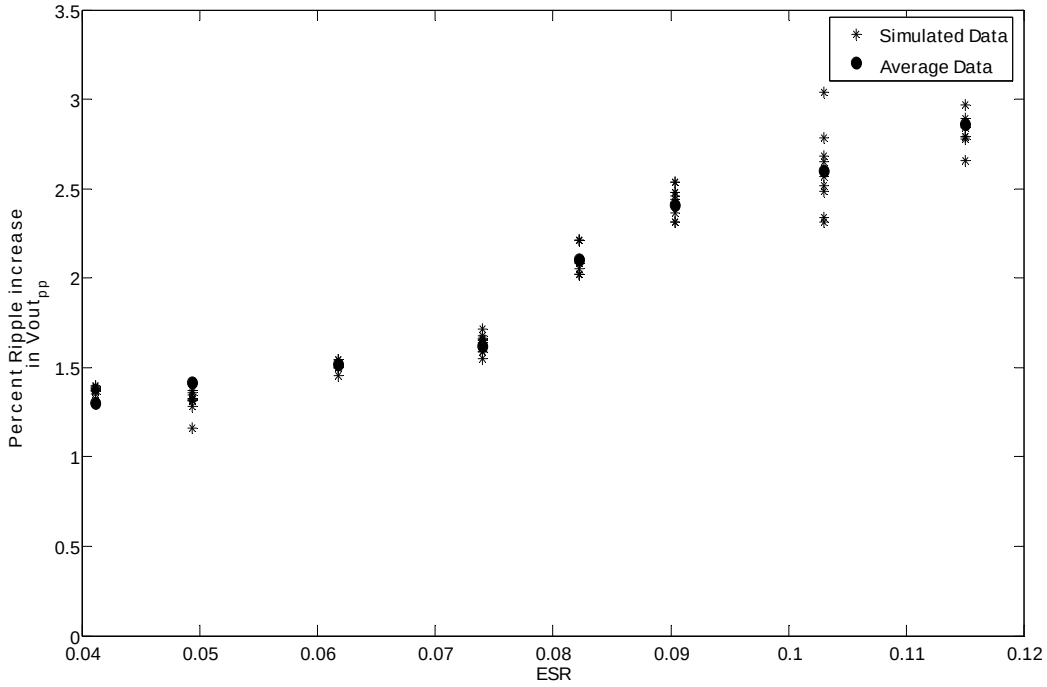

Figure 12: Percentage increase in the output ripple voltage

The plots in Figure 13 show the simulation results for output voltage of the DC-DC converter over time as the capacitor degrades. The plot indicates that the output voltage decreases to approximately 4.92 ± 0.013 V, i.e., a 2.8% decrease in output in 5000 operating hours. This plot helps us determine the rate at which the DC-DC converter degrades and the expected life of the converter under nominal operating conditions. From the simulation data we calculate the output voltage of DC-DC converter to drop at the rate of approximately 9μV/hr under the given operating conditions. This is taking into account industry standard specifications, which states that the output voltage ripple percentage for a DC-DC converter of 5V and less should not increase above 3-5% of the total voltage. This very much depends on the type of the application of the converters. Some have very stringent requirements while the rest can allow some higher percentage of output ripple voltage.

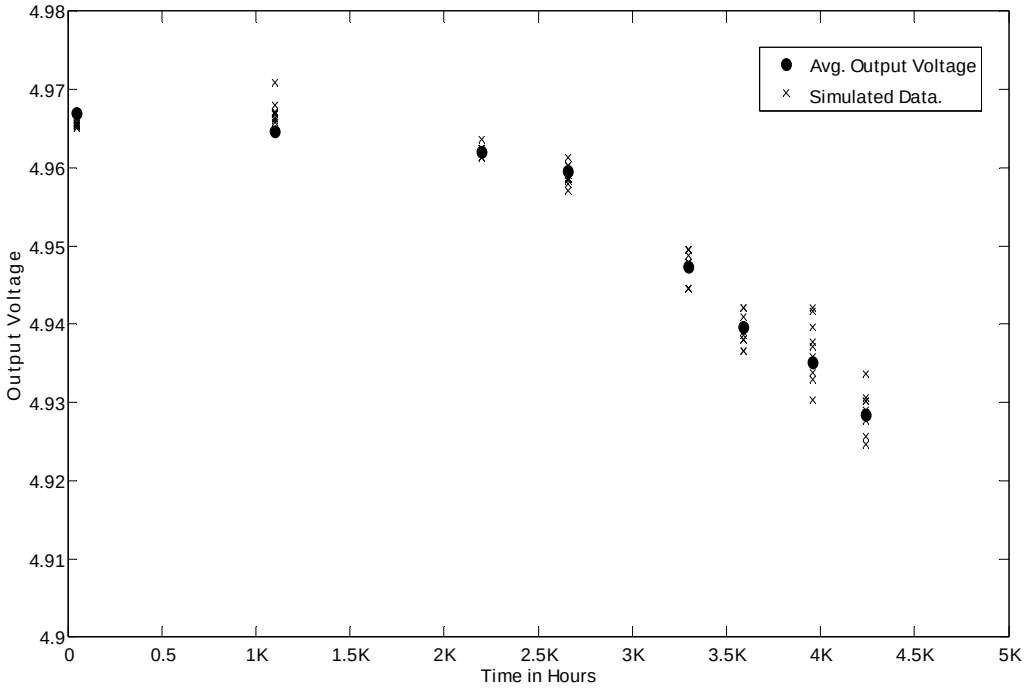

Figure 13: Output ripple voltage for DC-DC converter simulation.

We are presently conducting similar experiments as our simulation models to compare the actual experimental data with the recorded simulation data. Our future work will be conducting experiments and collecting data and matching with the model simulation data.

CONCLUSION:

This work discussed in the paper proposes a model-based approach to study electrolytic capacitor degradation in DC-DC converters. The physics of failure model derived expressed the change in ESR values as a function of time for given operating temperature conditions. According to industry standards, an electrolytic capacitor is considered unworthy of being used in the system when their ESR value exceeds 2.8 times its initial value. With our experiments we are developing a systematic method for predicting this ageing time of components. We will be able to recalculate some of the model parameters more accurately from the experimental data and improve the model. In the present work we conducted experiments under single operating conditions and parameter estimation for one of the component was considered. In future we plan to conduct experiments at different ambient temperature conditions and observe the degradation effect with respect to the increase in the ESR value of the capacitors.

These updated parameter estimation results for the model will help in predicting the failures and degradation in the capacitor elements with higher accuracy and precision. The work will provide a methodology for more accurate estimation of model parameters, and therefore, the capability to build more accurate degradation models.

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